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PATENT
U.S. Serial No. 09/336,090
Docket No. 0023-0115

IN THE SPECIFICATION:

Please amend the specification as follows:

Please replace the paragraph beginning at page 1, line 6, with the following:

--This application claims the benefit of priority under 35 U.S.C. 119(e) to US Provisional Application Serial No. 60/090,028, filed June 19, 1998, and is related to US Patent Application No. 09/237,128, filed January 25, 1999, and entitled "NETWORK PACKET FORWARDING LOOKUP WITH A REDUCED NUMBER OF MEMORY ACCESSES," US Patent Application No. 09/336,311, filed June 18, 1999, and entitled "A QUALITY OF SERVICE FACILITY IN A DEVICE FOR PERFORMING IP FORWARDING AND ATM SWITCHING," US Patent Application No. 09/336,229, filed June 18, 1999, and entitled "DEVICE FOR PERFORMING IP FORWARDING AND ATM SWITCHING," and US Patent Application No. 09/335,947, filed June 18, 1999, and entitled "METHOD AND SYSTEM FOR ENCAPSULATING/DECAPSULATING DATA ON A PER CHANNEL BASIS IN HARDWARE". The entire contents of each of the applications are hereby incorporated by reference.--

Q1

Please replace the paragraph beginning at page 3, line 17, with the following:

--Accordingly, in an aspect consistent with the principles of the invention, there is provided an interconnect network that enables a multi-service communication node to handle a variety of communication protocols, without requiring the maintenance of costly parallel networks.--

Q2

PATENT
U.S. Serial No. 09/336,090
Docket No. 0023-0115

Please replace the paragraph beginning at page 3, line 21, with the following:

Q3

--In accordance with another aspect consistent with the principles of the invention, there is provided an interconnect network that enables a communication node to adapt to communication protocols employed by emerging technologies.--

Please replace the paragraph beginning at page 3, line 25, with the following:

Q4

--In accordance with yet another aspect consistent with the principles of the invention, there is provided a scalable interconnect network enabling bandwidth scaling of a communication node to fit the needs of providers having varying bandwidth requirements.--

Please replace the paragraph beginning at page 3, line 29, with the following:

Q5

--In accordance with a further aspect consistent with the principles of the invention, there is provided a fault-tolerant interconnect network capable of repair and update, without causing down-time or compromising operation of the communication node.--

Please replace the paragraph beginning at page 4, line 1, with the following:

Q6

--These and other aspects of the invention will be described with respect to the following description of the invention.--

Please replace the paragraph beginning at page 11, line 27, with the following:

--Another feature of the invention is dynamic bandwidth scalability. A communication node employing interconnection networks according to an illustrative embodiment of the invention, employs a modular design. The modular design enables a service provider to change the number of communication channels by adding or subtracting physical proximately located modules to or from the communication node. According to one embodiment, the modules include a plurality of I/O interfaces coupled to an associated interconnection network. In a further embodiment of the invention, the communication node employs a two-level interconnection network modularity; a local level and an expanded level. More particularly, a plurality of local interconnection network modules, preferably proximately located with respect to each other, couple to an expanded interconnection network, also preferably located proximate to the local interconnection modules. By changing the number of local interconnection network modules that are "plugged-in" to the expanded interconnection module, a service provider can change the bandwidth of the communication node. Moreover, according to a further embodiment, a service provider can connect and unconnect local interconnect modules while the communication node is operating transferring information, thus, providing dynamic bandwidth scalability.--

Please replace the paragraph beginning at page 14, line 16, with the following:

--The local line card module 102 includes eight local line cards 202-216. Local line cards 202-216 are printed circuit boards holding integrated circuits and other components. Each line card 202-216 has six internal (I/O) ports 202a-202f, and an external SONET I/O port 202g. Line

card 202 couples information between external I/O port 202g and internal I/O ports 202a-202f. External I/O port 202g couples information into and out of the node 200, and the internal I/O ports 202a-202f connect with up to forty-eight internal communication lines and couple information between the local line card module 102 and the local interconnect module 118. Typically, each internal I/O port a-f includes a Gigabit Ethernet transceiver, providing a Gigabit Ethernet input channel and a Gigabit Ethernet output channel. Preferably, the input and output channels provide 10-bits of information. However, it should be noted that the term transceiver, as used throughout this description, is also intended to encompass structures including separate receivers and transmitters. The external I/O port 202g is preferably software configurable for either SONET or SDH operation. Thus, physical interfaces are software configurable for OC48 or STM16. SONET and SDH PAMS may be freely intermixed within access module 142. A fully loaded local line card module 102 can have up to eight external SONET/SDH I/O ports and forty-eight corresponding internal I/O ports.--

Please replace the paragraph beginning at page 20, line 13, with the following:

--In operation, and as illustrated in TABLE 1 above, the communication node 200 transfers each 16-byte group over a different internal communication channel. By way of example and referring again to FIGURE 3, assume each line card 202-216 has an associated address, and information enters line card 202 by way of external port 202g. Assume further that the entering information has a destination address of line card 208. As shown in FIGURE 2, internal port 202a couples a first 16-byte group to internal port 0a of interconnect board 218.

Internal port 202b couples a second 16-byte group to internal port 0b of board 218. Internal port 202c couples a third 16-byte group to internal port 0a of board 220, and internal port 202d couples a fourth 16-byte group to internal port 0b of board 220. Internal port 0a of board 218 couples the first 16-byte group to ASIC 224a. Internal port 0b of board 218 couples the second 16-byte group to ASIC 224b. Internal port 0a of board 220 couples the third 16-byte group to ASIC 226a, and internal port 0b of board 220 couples the fourth 16-byte group to ASIC 226b.--

Please replace the paragraph beginning at page 23, line 16, with the following:

--The expanded interconnect module 134 includes three essentially identical expanded interconnect boards 136-140. Each board 136-140 includes, among other components, one hundred and twenty-eight Gigabit Ethernet transceivers. Each board 136-140 also includes four ASICs 402-408, 410-416, and 418-424, respectively. ASICs 402-424 are essentially identical to ASICs 224-228. However, ASICs 402-424 are mode selected to operate in an expanded interconnect mode, rather than the local interconnect mode of ASICs 224-228. As in the case of ASICs 224-228, ASICs 402-424 each logically subdivides into an a-half and a b-half. Each half includes sixteen Gigabit Ethernet I/O ports, wherein each port includes a Gigabit input channel and a Gigabit output channel. Each of the sixteen Gigabit Ethernet ports couple to a Gigabit transceiver on the extended interconnect board.--

Please replace the paragraph beginning at page 23, line 28, with the following:

--By way of a specific example, board 136 of FIGURE 5 includes ASICs 402-408. ASIC 402 is subdivided into two logical halves 402a and 402b. Similarly, ASIC 404 is subdivided into logical halves 404a and 404b; ASIC 406 is subdivided into logical halves 406a and 406b; and ASIC 408 is subdivided into logical halves 408a and 408b. ASIC 402 includes Gigabit Ethernet ports 0a-15a, on half 402a, and 0b-15b on half 402b. Ports 0a-15a couple to transceivers 0-15 on board 136, and ports 0b-15b couple to transceivers 16-31. Gigabit ports 0a-15a and 0b-15b of ASICs 404-408 successively couple to remaining transceivers 32-127. Gigabit I/O ports of ASICs 410-416 and 418-424 couple to one hundred and twenty-eight transceivers of boards 138 and 140, respectively, in an identical fashion to that described with respect to ASICs 402-404 on board 136.--

Please replace the paragraph beginning at page 27, line 23, with the following:

--As discussed above in the Summary of the Invention, and as discussed in further detail below, according to a preferred embodiment, the invention employs a plurality of memory storage queues / buffers to aid in the efficient transfer of information. It should be noted that the terms queue and buffer are used interchangeably. The dual-port RAM 730 provides an output queue for each transceiver of sets 704 and 708. More specifically, information cells coupled into board 218 to be transferred to a line card 202-204 of local interconnect 102, are first written into buffer memory at an address which is written into an output queue. Free list memory 742 provides a list of available buffer memory addresses. There is a reference counter 744 for each of the 1536 buffers in the dual port RAM 730. Reference counter 744 contains the number of